Si5350B

FACTORY-PROGRAMMABLE ANY-FREQUENCY CMOS CLOCK GENERATOR + VCXO

Features

- Generates up to 8 non-integer-related frequencies from 8 kHz to 160 MHz
- Exact frequency synthesis at each output (0 ppm error)
- Highly linear VCXO gain (kv)
- Glitchless frequency changes
- Configurable Spread Spectrum selectable at each output
- User-configurable control pins:
  - Output Enable (OEB_0/1/2)
  - Power Down (PDN)
  - Frequency Select (FS_0/1)
  - Spread Spectrum Enable (SSEN)
- Supports static phase offset
- Rise/fall time control
- Operates from a low-cost, fixed frequency AT-cut, non-pullable crystal: 25 or 27 MHz
- Separate voltage supply pins:
  - Core VDD: 2.5 V or 3.3 V
  - Output VDDO: 2.5 V or 3.3 V
- Excellent PSRR eliminates external power supply filtering
- Low output period jitter: 100 ps pp
- Very low power consumption (<40 mA)
- Available in 3 packages types:
  - 10-MSOP: 3 outputs
  - 24-QSOP: 8 outputs
  - 20-QFN (4x4 mm): 8 outputs
- PCIE Gen 1 compliant
- Supports HCSL compatible swing

10-MSOP



24-QSOP



20-QFN



Ordering Information:

See page 19

Applications

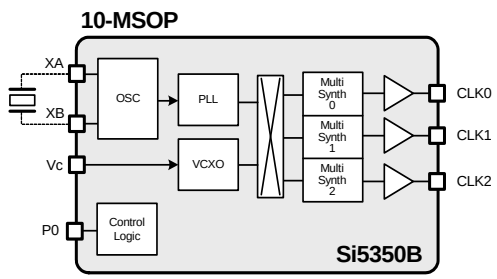
- HDTV, DVD/Blu-ray, set-top box
- Audio/video equipment, gaming
- Printers, scanners, projectors
- Residential gateways
- Networking/communication
- Servers, storage
- XO replacement

Description

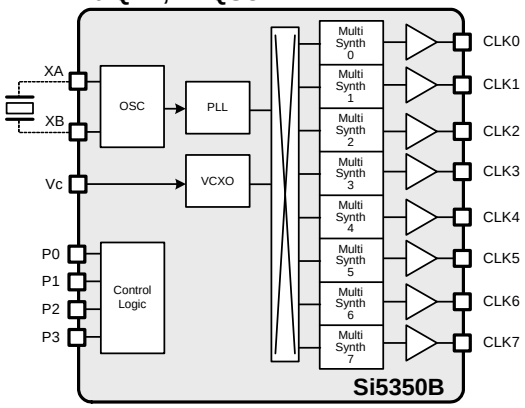
The Si5350B combines a clock generator and VCXO function into a single device. A flexible architecture enables this user definable custom timing device to generate any of the specified output frequencies from either the internal PLL or the VCXO. This allows the Si5350B to replace multiple crystals, crystal oscillators, and VCXOs. Custom pin-controlled Si5350B devices are requested using the ClockBuilder web-based utility (www.silabs.com/ClockBuilder).

Functional Block Diagram

10-MSOP



20-QFN, 24-QSOP



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This information applies to a product under development. Its characteristics and specifications are subject to change without notice.

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1. Electrical Specifications

Table 1. Recommended Operating Conditions

(V_{DD} = 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature	T_A		–40	25	85	°C
Core Supply Voltage	V_{DD}		3.0	3.3	3.60	V
			2.25	2.5	2.75	V
Output Buffer Voltage	V_{DDOx}		2.25	2.5	2.75	V
			3.0	3.3	3.60	V
Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.						

Table 2. DC Characteristics

(V_{DD} = 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Core Supply Current*	I_{DD}	Enabled 3 outputs	—	20	30	mA
		Enabled 8 outputs	—	25	40	mA
		Power Down (PDN = V_{DD})	—	—	15	µA
Output Buffer Supply Current (Per Output)*	I_{DDOx}	C_L = 5 pF	—	2.0	4.5	mA
Input Current	I_{P0-P3}	Pins P0, P1, P2, P3 Vin < 3.6 V	—	—	10	µA
	I_{VC}	VC	—	—	30	µA
Output Impedance	Z_{OI}	8 mA output drive current, see Design Considerations section	—	85	—	Ω
***Note:** Output clocks less than or equal to 133 MHz.						

Table 3. AC Characteristics

(V_{DD} = 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VCXO Control Voltage Range	Vc		0	$V_{DD}/2$	V_{DD}	V
VCXO Gain (configurable)	kv	Vc = 10–90% of V_{DD}	18	—	150	ppm/V
VCXO Control Voltage Linearity	KVL	Vc = 10–90% of V_{DD}	–5	—	+5	%
VCXO Pull Range (configurable)*	PR	V_{DD} = 3.3 V Vc = 10–90% of V_{DD}	±30	0	±240	ppm
VCXO Modulation Bandwidth			—	10	—	kHz
Power-Up Time	TRDY	From V_{DD} = V_{DDmin} to valid output clock, C_L = 5 pF, f_{CLKn} > 1 MHz	—	2	10	ms
Power-Down Time	T_{PD}	From V_{DD} = V_{DDmin}, C_L = 5 pF, f_{CLKn} > 1 MHz	—	5	100	ms
Output Enable Time	T_{OE}	From OEB assertion to valid clock output, C_L = 5 pF, f_{CLKn} > 1 MHz	—	—	10	µs
Output Frequency Transition Time	T_{FREQ}	f_{CLKn} > 1 MHz	—	—	10	µs
Spread Spectrum Frequency Deviation	SS_{DEV}	Down spread	–0.5	—	–2.5	%
Spread Spectrum Modulation Rate	SS_{MOD}		30	31.5	33	kHz
***Note:** Contact Silicon Labs for VCXO operation at 2.5 V.						

Table 4. Input Characteristics

(V_{DD} = 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
VC Input Resistance			100	—	—	kΩ
P0-P3 Input Low Voltage	VIL-P0-3		–0.1	—	0.3 x V_{DD}	V
P0-P3 Input High Voltage	VIH_P0-3		0.7 x V_{DD}	—	3.60	V

Table 5. Output Characteristics

(V_{DD} = 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Frequency Range	FCLK		0.008	—	160	MHz
Load Capacitance	C_L	F_{CLK} < 100 MHz	—	—	15	pF
Duty Cycle	DC	Measured at $V_{DD}/2$	45	50	55	%
Rise/Fall Time	t_r/t_f	20% - 80%, C_L = 5 pF	0.5	1	1.5	ns
Output High Voltage	VOH		V_{DD} – 0.6	—	—	V
Output Low Voltage	VOL		—	—	0.6	V
Period Jitter	JPER	Measured over 10k cycles	—	60	100	ps pk-pk
Period Jitter, VCXO	JPER_VCXO		—	60	110	ps pk-pk
Cycle-to-Cycle Jitter	JCC	Measured over 10k cycles	—	50	90	ps pk
Cycle-to-Cycle Jitter, VCXO	JCC_VCXO		—	50	95	ps pk
RMS Phase Jitter	JRMS	12 kHz–20 MHz	—	3.5	11	ps
RMS Phase Jitter	JRMS_VCXO		—	8.5	18.5	ps rms

Table 6. 25 MHz Crystal Requirements[1,2]

Parameter	Symbol	Min	Typ	Max	Unit
Crystal Frequency	f_{XTAL}	—	25	—	MHz
Load Capacitance	C_L	6	—	12	pF
Equivalent Series Resistance	r_{ESR}	—	—	150	Ω
Crystal Max Drive Level	d_L	—	—	100	µW

Notes:

1. Crystals which require load capacitances of 6, 8, or 10 pF should use the device's internal load capacitance for optimum performance. See register 183 bits 7:6. A crystal with a 12 pF load capacitance requirement should use a combination of the internal 10 pF load capacitors in addition to external 2 pF load capacitors. Adding external 2 pF load capacitors can minimize jitter by 20%.
2. Refer to "AN551: Crystal Selection Guide" for more details.

Table 7. 27 MHz Crystal Requirements[1,2]

Parameter	Symbol	Min	Typ	Max	Unit
Crystal Frequency	f_{XTAL}	—	27	—	MHz
Load Capacitance	C_L	6	TBD	12	pF
Equivalent Series Resistance	r_{ESR}	—	—	150	Ω
Crystal Max Drive Level Spec	d_L	—	—	100	µW

Notes:
1. Crystals which require load capacitances of 6, 8, or 10 pF should use the device's internal load capacitance for optimum performance. See register 183 bits 7:6. A crystal with a 12 pF load capacitance requirement should use a combination of the internal 10 pF load capacitors in addition to external 2 pF load capacitors. Adding external 2 pF load capacitors can minimize jitter by 20%.
2. Refer to "AN551: Crystal Selection Guide" for more details.

Table 8. Thermal Characteristics

Parameter	Symbol	Test Condition	Package	Value	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	10-MSOP	131	°C/W
			24-QSOP	80	°C/W
			20-QFN	51	°C/W
Thermal Resistance Junction to Case	θ_{JC}	Still Air	10-MSOP	43	°C/W
			24-QSOP	31	°C/W
			20-QFN	16	°C/W

Table 9. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Value	Unit
DC Supply Voltage	V_{DD_max}		–0.5 to 3.8	V
Input Voltage	VIN_P0-3	Pins P0, P1, P2, P3	–0.5 to 3.8	V
	VIN_VC	VC	–0.5 to (VDD+0.3)	V
	VIN_XA/B	Pins XA, XB	–0.5 to 1.3 V	V
Temperature Range	T_J		–55 to 150	°C

Note: Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Typical Application

2.1. Si5350B Replaces Multiple Clocks and XOs

The Si5350B is a clock generation device that provides both synchronous and free-running clocks for applications where power, board size, and cost are critical. An application where both free-running and synchronous clocks are required is shown in Figure 1.

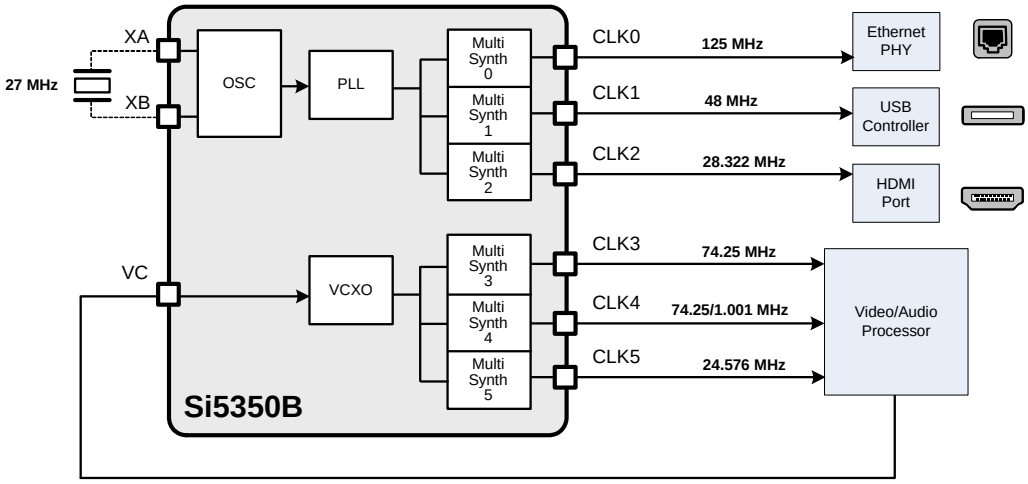
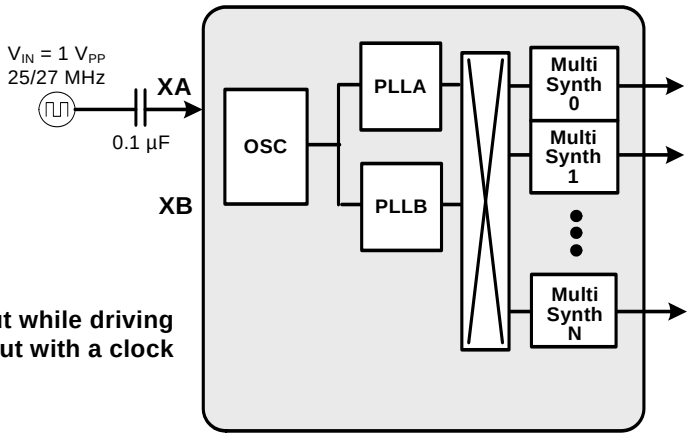


Figure 1. Example of an Si5350B in an Audio/Video Application

2.2. Replacing a Crystal with a Clock

The Si5350B can be driven with a clock signal through the XA input pin.



Note: Float the XB input while driving the XA input with a clock

Figure 2. Si5350B Driven by a Clock Signal

2.3. HCSL Compatible Outputs

The Si5350B can be configured to support HCSL compatible swing when the VDDO of the output pair of interest is set to 2.5 V (i.e., VDDOA must be 2.5 V when using CLK0/1; VDDOB must be 2.5 V for CLK2/3 and so on).

The circuit in the figure below must be applied to each of the two clocks used, and one of the clocks in the pair must also be inverted to generate a differential pair.

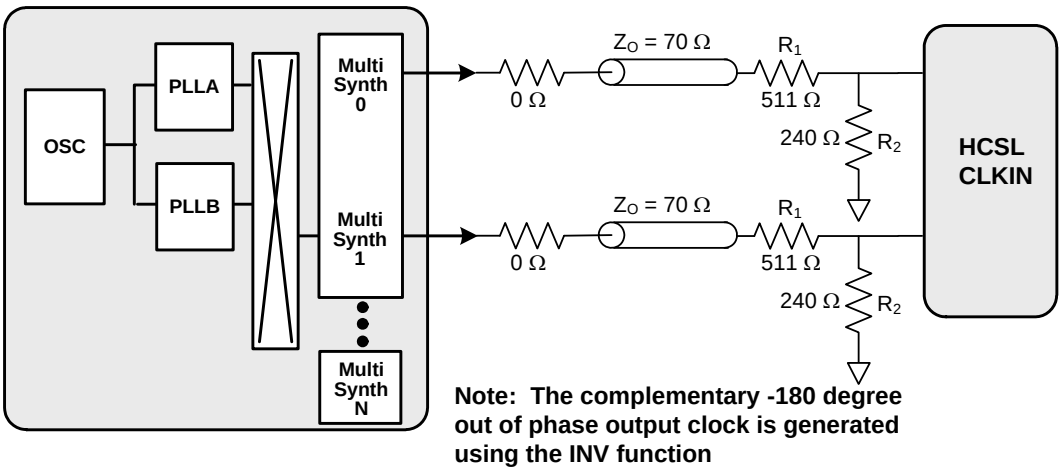


Figure 3. Si5350B Output is HCSL Compatible

3. Functional Description

The Si5350B features a high-frequency PLL, a high-frequency VCXO and a high-resolution fractional MultiSynth™ divider on each output. A block diagram of both the 3-output and the 8-output clock generators are shown in Figure 4. Free-running clocks are generated from the on-chip oscillator + PLL, and a separate voltage controlled oscillator (VCXO) is used to generate synchronous clocks. A fixed-frequency non-pullable standard AT-cut crystal provides frequency stability for both the internal oscillator and VCXO. The flexible synthesis architecture of the Si5350B generates up to eight non-integer related frequencies and any combination of free-running and/or synchronous clocks.

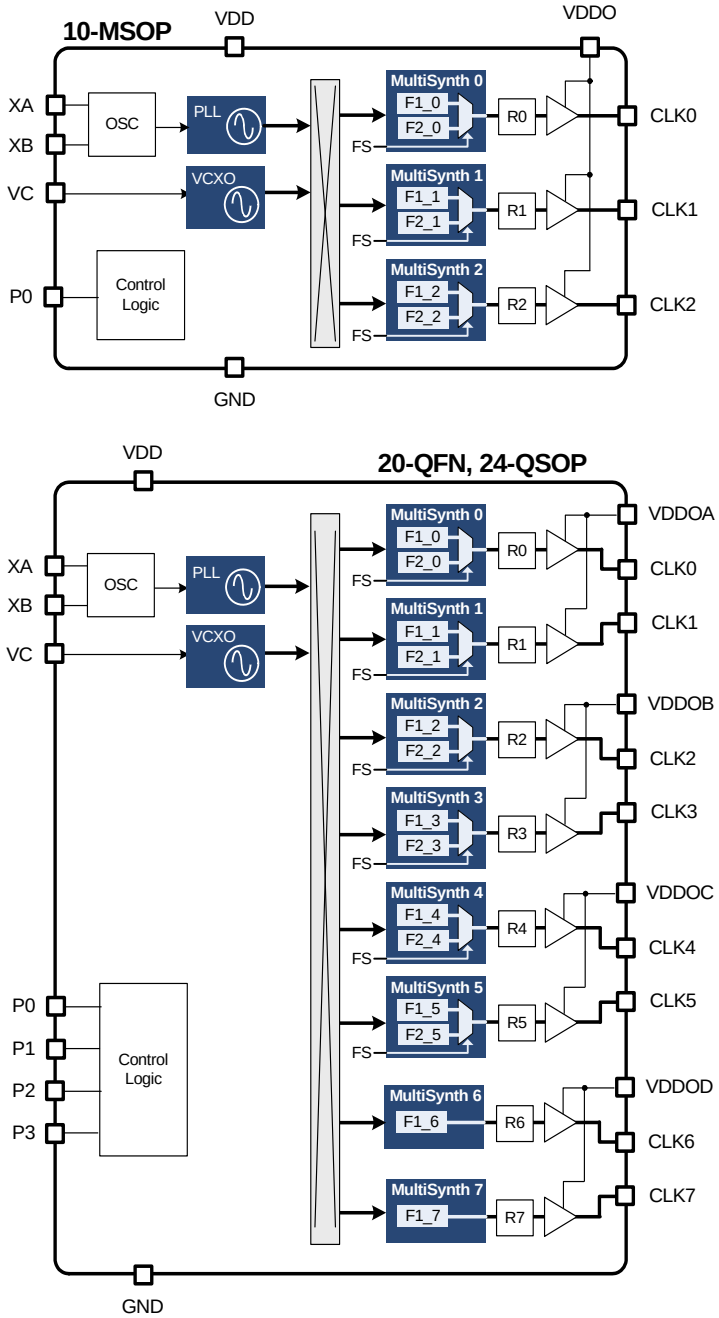


Figure 4. Block Diagram of the 3 and 8 Output Si5350B Devices

4. Configuring the Si5350B

The Si5350B is a factory-programmed custom clock generator that is user definable with a simple to use web-based utility (www.silabs.com/ClockBuilder). The ClockBuilder utility provides a simple graphical interface that allows the user to enter input and output frequencies along with other custom features as described in the following sections. All synthesis calculations are automatically performed by ClockBuilder to ensure an optimum configuration. A unique part number is assigned to each custom configuration.

4.1. Crystal Inputs (XA, XB)

The Si5350B uses a fixed-frequency non-pullable standard AT-cut crystal as a reference to synthesize its output clocks and to provide the frequency stability for the VCXO.

4.1.1. Crystal Frequency

The Si5350B can operate using either a 25 MHz or a 27 MHz crystal.

4.1.2. Internal XTAL Load Capacitors

Internal load capacitors (C_L) are provided to eliminate the need for external components when connecting a XTAL to the Si5350B. Options for internal load capacitors are 6, 8, or 10 pF. XTALs with alternate load capacitance requirements are supported using external load capacitors ≤ 2 pF as shown in Figure 5.

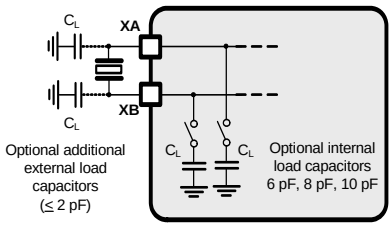


Figure 5. External XTAL with Optional Load Capacitors

4.2. Output Clocks (CLK0–CLK7)

The Si5350B is orderable as a 3-output (10-MSOP) or 8-output (24-QSOP, 20-QFN) clock generator. Output clocks CLK0 to CLK5 can be ordered with two clock frequencies (F1_x, F2_x) which are selectable with the optional frequency select pins (FS0/1). See “4.3.2. Frequency Select (FS_0, FS_1)” for more details on the operation of the frequency select pins. Each output clock can select its reference either from the PLL or from the VCXO.

4.2.1. Output Clock Frequency

Outputs can be configured at any frequency from 8 kHz up to 100 MHz. In addition, the device can generate any two non-integer related frequencies up to 160 MHz. See “AN554: Si5350/51 PCB Layout Guide” for details.

4.2.2. .Spread Spectrum

Spread spectrum can be enabled on any of the clock outputs that use PLLA as its reference. Spread spectrum is useful for reducing electromagnetic interference (EMI). Enabling spread spectrum on an output clock modulates its frequency, which effectively reduces the overall amplitude of its radiated energy. See AN554 for details. Note that spread spectrum is not available on clocks synchronized to PLLB or to the VCXO.

The Si5350B supports several levels of spread spectrum allowing the designer to choose an ideal compromise between system performance and EMI compliance. An optional spread spectrum enable pin (SSEN) is configurable to enable or disable the spread spectrum feature. See “4.3.1. Spread Spectrum Enable (SSEN)” for details.

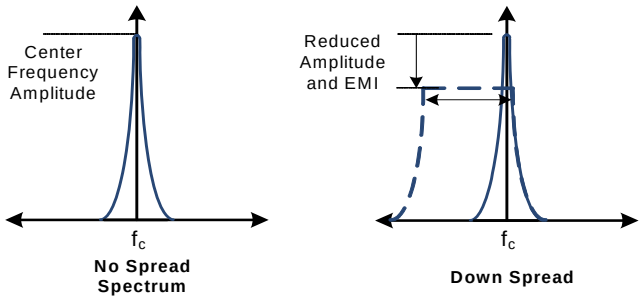


Figure 6. Available Spread Spectrum Profiles

4.2.3. Invert/Non-Invert

By default, each of the output clocks are generated in phase (non-inverted) with respect to each other. An option to invert any of the clock outputs is also available.

4.2.4. Output State When Disabled

There are up to three output enable pins configurable on the Si5350B as described in “5. Pin Descriptions (20-QFN, 24-QSOP)” . The output state when disabled for each of the outputs is configurable as one of the following: disable low, disable high, or disable in high-impedance.

4.2.5. Powering Down Unused Outputs

Unused clock outputs can be completely powered down to conserve power.

4.3. Programmable Control Pins (P0–P3) Options

Up to four programmable control pins (P0-P3) are configurable allowing direct pin control of the following features:

4.3.1. Spread Spectrum Enable (SSEN)

An optional control pin allows disabling the spread spectrum feature for all outputs that were configured with spread spectrum enabled. Hold SSEN low to disable spread spectrum. The SSEN pin provides a convenient method of evaluating the effect of using spread spectrum clocks during EMI compliance testing.

4.3.2. Frequency Select (FS_0, FS_1)

The Si5350B offers the option of configuring up to two frequencies per clock output (CLK0-CLK5) for either free-running or synchronous clocks. This is a useful feature for applications that need to support more than one free-running or synchronous clock rate on the same output. An example of this is shown in Figure 7. The FS pins select which frequency is generated from the clock output. In this example FS0 select the output frequency on CLK0, and FS1 selects the frequency on CLK1.

FS0 Bit Level	Free-running Frequency	
0	F1_0:	74.25 MHz
1	F2_0:	$\frac{74.25}{1.001}$ MHz

FS1 Bit Level	Synchronous Frequency	
0	F1_1:	24.576 MHz
1	F2_1:	22.5792 MHz

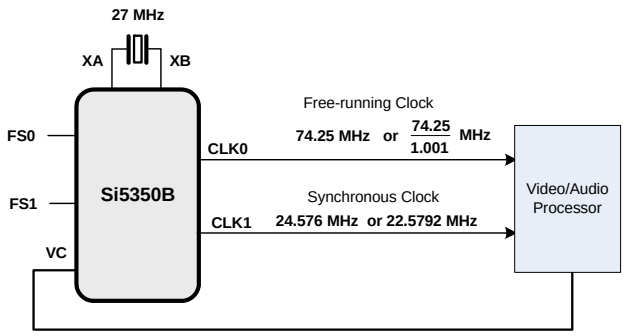


Figure 7. Example of Generating Two Clock Frequencies from the Same Clock Output

Up to two frequency select pins are available on the Si5350B. Each of the frequency select pins can be linked to any of the clock outputs as shown in Figure 8. For example, FS_0 can be linked to control clock frequency selection on CLK0, CLK3, and CLK5; FS_1 can be used to control clock frequency selection on CLK1, CLK2, and CLK4. Any other combination is also possible.

The Si5350B uses control circuitry to ensure that frequency changes are glitchless. This ensures that the clock always completes its last cycle before starting a new clock cycle of a different frequency.

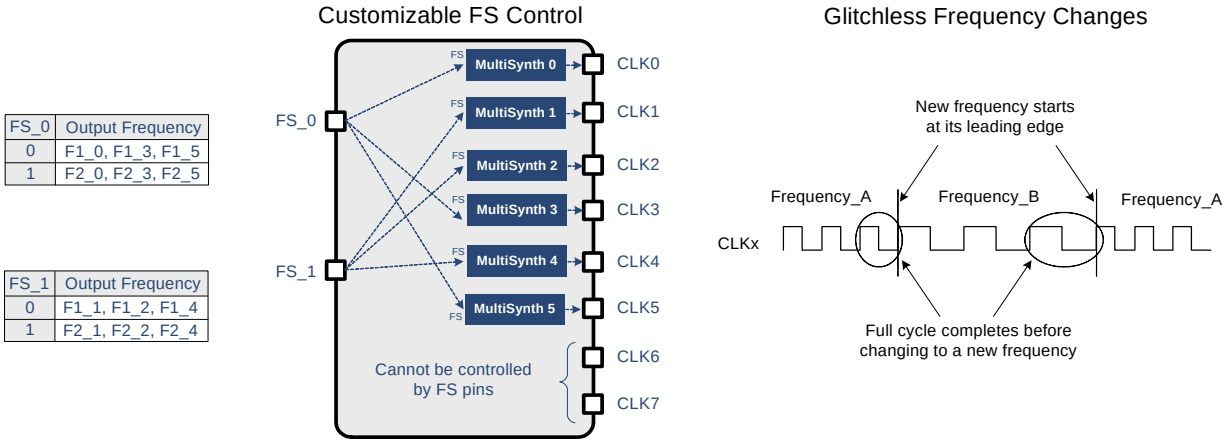


Figure 8. Example Configuration of a Pin-Controlled Frequency Select (FS)

4.3.3. Output Enable (OEB_0, OEB_1, OEB_2)

Up to three output enable pins (OEB_0/1/2) are available on the Si5350B. Similar to the FS pins, each OEB pin can be linked to any of the output clocks. In the example shown in Figure 9, OEB_0 is linked to control CLK0, CLK3, and CLK5; OEB_1 is linked to control CLK6 and CLK7, and OEB_2 is linked to control CLK1, CLK2, CLK4, and CLK5. Any other combination is also possible. If more than one OEB pin is linked to the same CLK output, the pin forcing a disable state will be dominant. Clock outputs are enabled when the OEB pin is held low.

The output enable control circuitry ensures glitchless operation by starting the output clock cycle on the first leading edge after OEB is asserted (OEB = low). When OEB is released (OEB = high), the clock is allowed to complete its full clock cycle before going into a disabled state. This is shown in Figure 9. When disabled, the output state is configurable as disabled high, disabled low, or disabled in high-impedance.

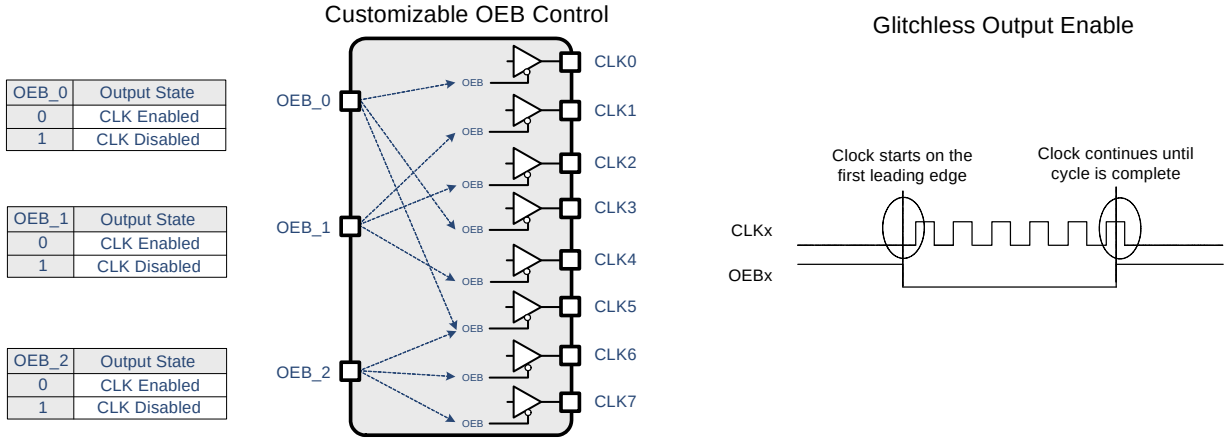


Figure 9. Example Configuration of a Pin-Controlled Output Enable

4.3.4. Power Down (PDN)

An optional power down control pin allows a full shutdown of the Si5350B to minimize power consumption when its output clocks are not being used. The Si5350B is in normal operation when the PDN pin is held low and is in power down mode when held high. Power consumption when the device is in power down mode is indicated in Table 2 on page 4.

4.4. Voltage Control Input (VC)

The VCXO architecture of the Si5350B eliminates the need for an external pullable crystal. Only a standard, low-cost, fixed-frequency (25 or 27 MHz) AT-cut crystal is required.

The tuning range of the VCXO is configurable allowing for a wide variety of applications. Key advantages of the VCXO design in the Si5351 include high linearity, a wide operating range (linear from 10 to 90% of VDD), and reliable startup and operation. Refer to Table 3 on page 5 for VCXO specification details.

A unique feature of the Si5350B is its ability to generate multiple output frequencies controlled by the same control voltage applied to the VC pin. This replaces multiple PLLs or VCXOs that would normally be locked to the same reference. An example is illustrated in Figure 10.

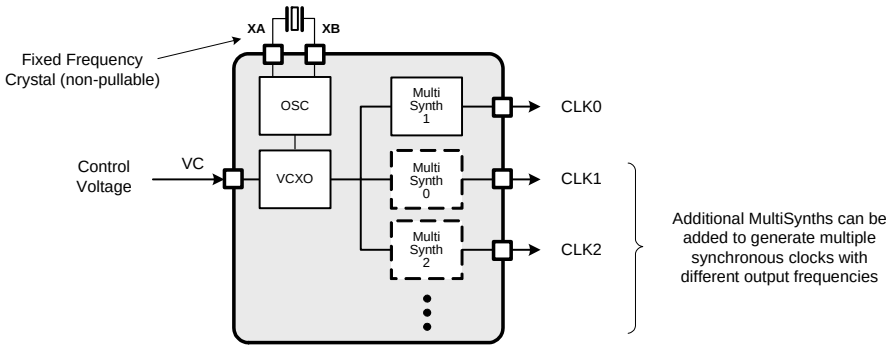


Figure 10. Generating One Or More Synchronous Clocks

4.4.1. Control Voltage Gain (kV)

The voltage level on the VC pin directly controls the output frequency. The rate of change in output clock frequency (kv) is configurable from 18 ppm/V up to 150 ppm/V. This allows a configurable pull range from ±30 ppm to ±150 ppm @ V_{DD} = 3.3 V as shown in Figure 11. Consult the factory for other pull range values.

A key advantage of the VCXO design in the Si5350B is its highly linear tuning range. This allows better control of PLL stability and jitter performance over the entire control voltage range.

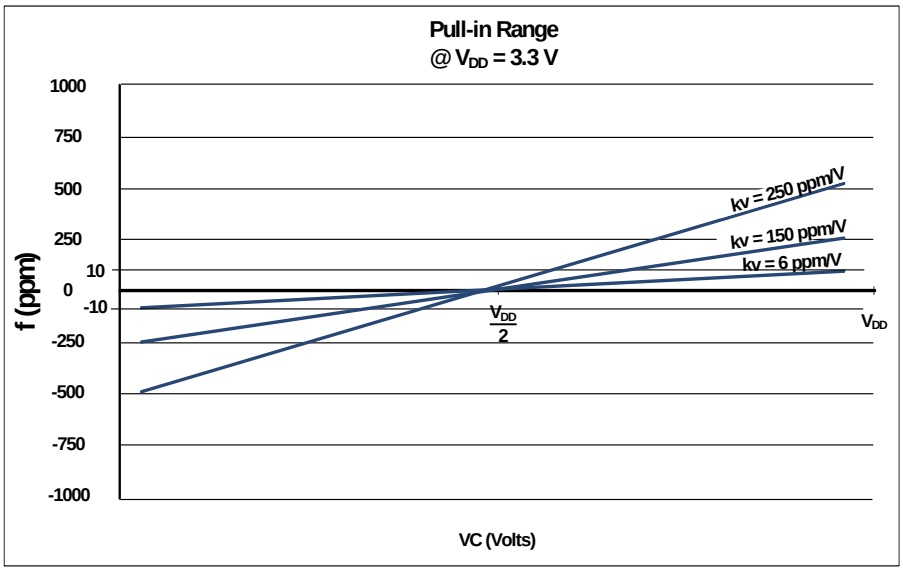


Figure 11. User-definable VCXO Pull Range

4.5. Design Considerations

The Si5350B is a self-contained clock generator that requires very few external components. The following general guidelines are recommended to ensure optimum performance.

4.5.1. Power Supply Decoupling/Filtering

The Si5350B has built-in power supply filtering circuitry to help keep the number of external components to a minimum. All that is recommended is one 0.1 µF decoupling capacitor per power supply pin. This capacitor should be mounted as close to the VDD and VDDO pins as possible without using vias.

4.5.2. Power Supply Sequencing

The VDD and VDDOx (i.e., VDDO0, VDDO1, VDDO2, VDDO3) power supply pins have been separated to allow flexibility in output signal levels. It is important that power is applied to all supply pins (VDD, VDDOx) at the same time. Unused VDDOx pins should be tied to VDD.

4.5.3. External Crystal

The external crystal should be mounted as close to the pins as possible using short PCB traces. The XA and XB traces should be kept away from other high-speed signal traces. See “AN551: Crystal Selection Guide” for more details.

4.5.4. External Crystal Load Capacitors

The Si5350B provides the option of using internal and external crystal load capacitors. If external load capacitors are used, they should be placed as close to the XA/XB pads as possible. See “AN551: Crystal Selection Guide” for more details.

4.5.5. Unused Pins

Unused control pins (P0–P4) should be tied to GND.

Unused voltage control pin should be tied to GND.

Unused output pins (CLK0–CLK7) should be left floating.

4.5.6. Trace Characteristics

The Si5350B features various output current drives ranging from 2 to 8 mA (default). It is recommended to configure the trace characteristics as shown in Figure 12 when an output drive setting of 8 mA is used.

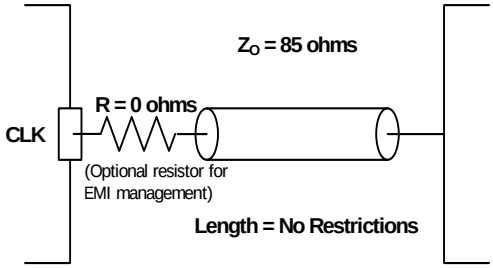
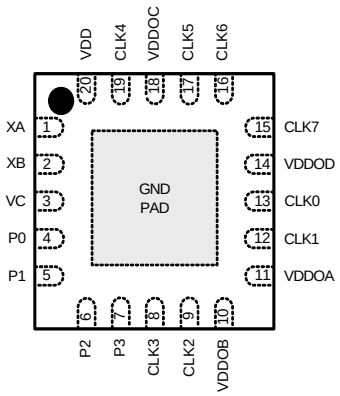


Figure 12. Recommended Trace Characteristics with 8 mA Drive Strength Setting

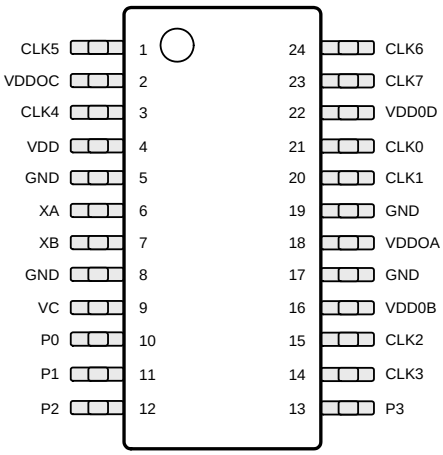
Note: Jitter is only specified at 6 and 8 mA drive strength.

5. Pin Descriptions (20-QFN, 24-QSOP)

Si5350B 20-QFN
Top View



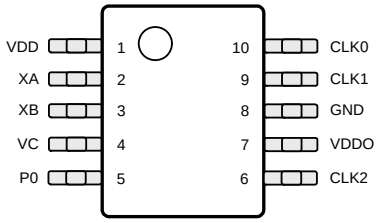
Si5350B 24-QSOP
Top View



Pin Name	Pin Number		Pin Type*	Function
	QFN-20	QSOP-24		
XA	1	6	I	Input pin for external XTAL
XB	2	7	I	Input pin for external XTAL
VC	3	9	I	VCXO control voltage input
CLK0	13	21	O	Output clock 0
CLK1	12	20	O	Output clock 1
CLK2	9	15	O	Output clock 2
CLK3	8	14	O	Output clock 3
CLK4	19	3	O	Output clock 4
CLK5	17	1	O	Output clock 5
CLK6	16	24	O	Output clock 6
CLK7	15	23	O	Output clock 7
P0	4	10	I	User configurable input pin 0
P1	5	11	I	User configurable input pin 1
P2	6	12	I	User configurable input pin 2
P3	7	13	I	User configurable input pin 3
VDD	20	4	P	Core voltage supply pin
VDDOA	11	18	P	Output voltage supply pin for CLK0 and CLK1
VDDOB	10	16	P	Output voltage supply pin for CLK2 and CLK3
VDDOC	18	2	P	Output voltage supply pin for CLK4 and CLK5
VDDOD	14	22	P	Output voltage supply pin for CLK6 and CLK7
GND	Center Pad	5, 8, 17, 19	P	Ground
***Note:** Pin Types: I = Input, O = Output, P = Power.				

6. Pin Descriptions (10-Pin MSOP)

Si5350B 10-MSOP
Top View



Pin Name	Pin Number	Pin Type*	Function
	MSOP-10		
XA	2	I	Input pin for external XTAL
XB	3	I	Input pin for external XTAL
Vc	4	I	VCXO control voltage input
CLK0	10	O	Output clock 0
CLK1	9	O	Output clock 1
CLK2	6	O	Output clock 2
P0	5	I	User configurable input pin 0
VDD	1	P	Core voltage supply pin
VDDO	7	P	Output supply pin for CLK0, CLK1, and CLK2
GND	8	P	Ground
***Note:** Pin Types: I = Input, O = Output, P = Power.			

7. Ordering Information

Factory programmed Si5350B devices can be requested using the ClockBuilder web-based utility available at: www.silabs.com/ClockBuilder. A unique part number is assigned to each custom configuration as indicated in Figure 13.

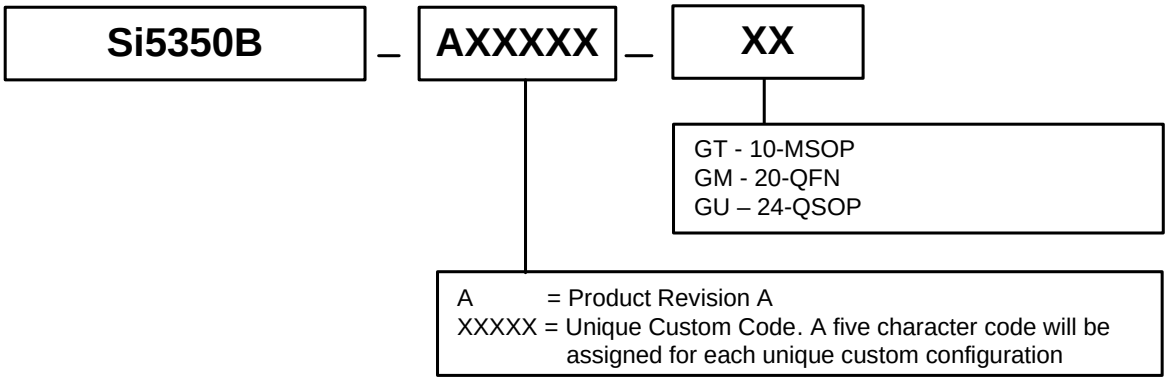


Figure 13. Custom Clock Part Numbers

An evaluation kit containing ClockBuilder Desktop software and hardware allows easy evaluation of the Si5350B.

8. Package Outline (24-Pin QSOP)

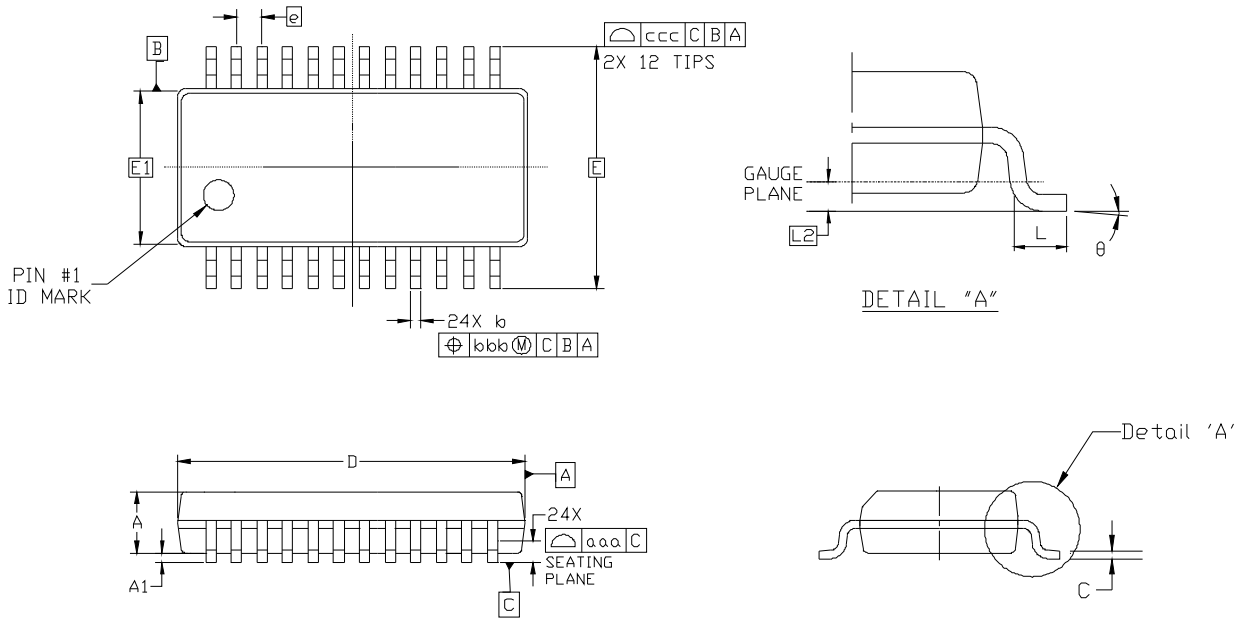


Table 10. 24-QSOP Package Dimensions

Dimension	Min	Nom	Max
A	—	—	1.75
A1	0.10	—	0.25
b	0.19	—	0.30
c	0.15	—	0.25
D	8.55	8.65	8.75
E		6.00 BSC	
E1	3.81	3.90	3.99
e		0.635 BSC	
L	0.40	—	1.27
L2		0.25 BSC	
θ	0	—	8
aaa		0.10	
bbb		0.17	
ccc		0.10	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-137, Variation C.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9. Package Outline (20-Pin QFN)

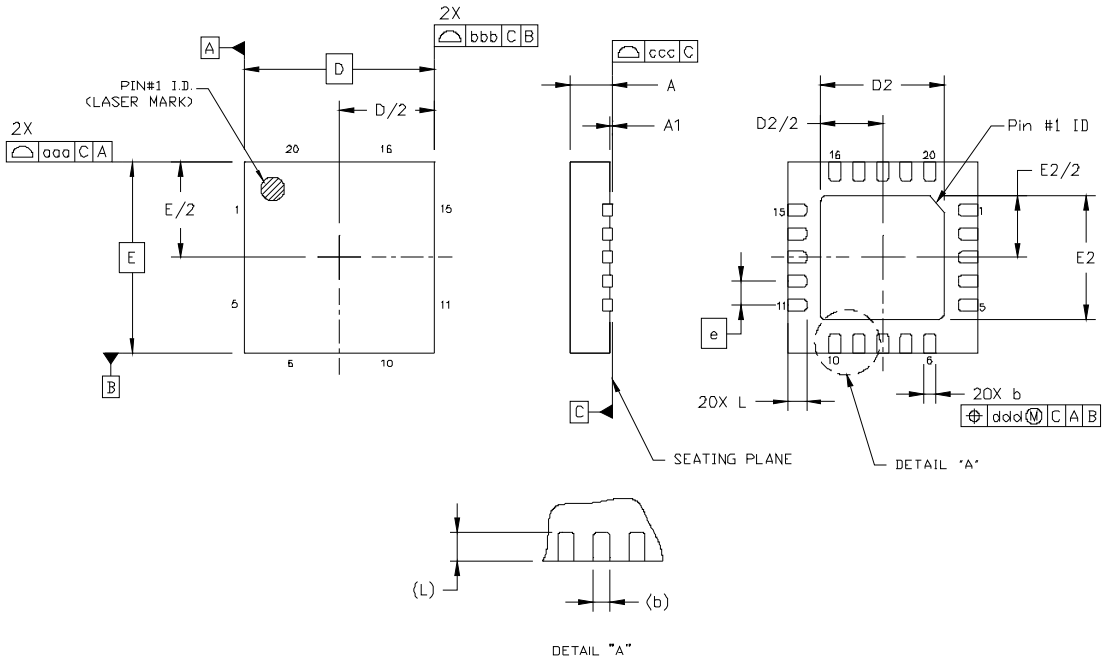


Table 11. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		4.00 BSC	
D2	2.65	2.70	2.75
e		0.50 BSC	
E		4.00 BSC	
E2	2.65	2.70	2.75
L	0.30	0.40	0.50
aaa			0.10
bbb			0.10
ccc			0.08
ddd			0.10
eee			0.10

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Outline MO-220, variation VGGD-8.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10. Package Outline (10-Pin MSOP)

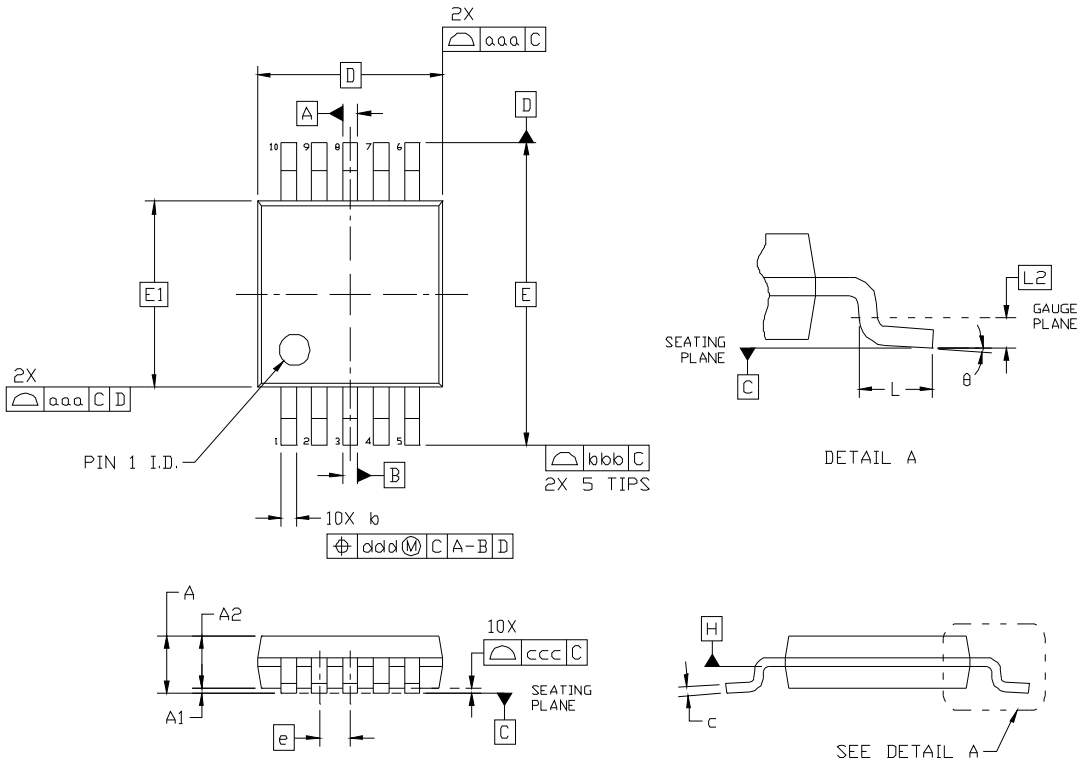


Table 12. 24-QSOP Package Dimensions

Dimension	Min	Nom	Max
A	—	—	1.10
A1	0.00	—	0.15
A2	0.75	0.85	0.95
b	0.17	—	0.33
c	0.08	—	0.23
D	3.00 BSC		
E	4.90 BSC		
E1	3.00 BSC		
e	0.50 BSC		
L	0.40	0.60	0.80
L2	0.25 BSC		
q	0	—	8
aaa	—	—	0.20
bbb	—	—	0.25
ccc	—	—	0.10
ddd	—	—	0.08

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-137, Variation C
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

DOCUMENT CHANGE LIST

Revision 0.2 to Revision 0.9

- Updated maximum output frequency.
- Updated kV values in Table 3 on page 5.
- Added "2.3. HCSL Compatible Outputs" on page 9.
- Updated "4.2.2. .Spread Spectrum" on page 11.
- Added "4.5.6. Trace Characteristics" on page 15.

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